FIG.1

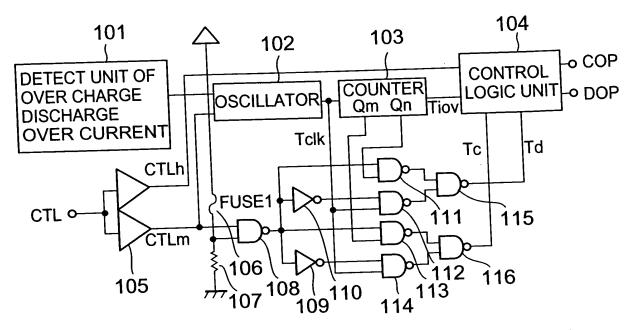
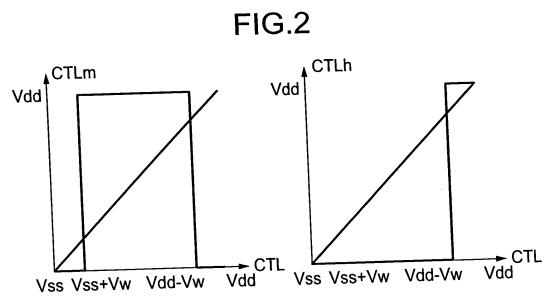


DIAGRAM SHOWING EMBODIMENT OF PRESET INVENTION



SIGNALS CTLm AND CTLh DUE TO VOLTAGE APPLIED TO TERMINAL CTL

